On page 23, line 22, please replace "cycle (164), which causes xfr to be low" to --cycle (166), and causes xfr to be low (168)--.

On page 24, line 1, please replace "during the second timing cycle and xfrA to be low (170) during a third timing cycle" with --during the second timing cycle. The assertion of holdA at 168 causes xfrA to be low (170) during a third timing cycle--.

IN THE DRAWING FIGURES

Amendment to FIGURES 11 and 14 are included herein. Please see the attached clean drawing sheets and marked-up drawing sheets for FIGURES 11 and 14.

REMARKS

The amendments to the specification, drawing Figures and claims 2, 3, and 4 are being submitted herewith to cure informalities discovered by the Applicants' Attorney upon further review of the present application. These amendments are being submitted though the present preliminary amendment in an earnest effort to advance this case to issue without delay. The Applicants respectfully request consideration of the present application as amended.

Charge Deposit Account

Please charge our Deposit Account No. 02-2666 for any additional fee(s) that may be due in this matter, and please credit the same deposit account for any overpayment.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: March 27, 2001

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Version of Amended Claims with Markings

2. The MAC bus interface of claim 1, wherein the first set of handshake signals corresponding to the data out bus comprise:

a request signal sent from the system side block to the network side block that is used to request a transfer of data to the network side block;

a transfer ready signal from the network side block to the system side block that is asserted by the network side block to inform the system side block that the network side block [is ready to receive data] has accepted a portion of data presented by the system side block for transfer; and

a hold signal issued sent from the system side block to the network side block that may be asserted to control a timing of the transfer of data.

3. The MAC bus interface of claim 1, wherein the second set of handshake signals corresponding to the out message bus comprise:

a message request signal from the network side block to the system side block that is used to request a transfer of the message data from the network side block to the system side block; and

a message transfer ready signal asserted by the system side block to inform the network side block that the [message data may be received by the system side block] system side block has accepted a portion of data presented by the network side block for transfer.

4. The MAC bus interface of claim 1, wherein the third set of handshake signals corresponding to the data in bus comprise:

a request signal sent from the network side block to the system side block that is used to request a transfer of data to the system side block;

a transfer ready signal sent from the system side block to the network side block that is asserted by the system side block to inform the network side block that the system side block [is ready to receive data] has accepted a portion of data presented by the network side block for transfer; and

a hold signal issued from the network side block to the system side block that may be asserted to control a timing of the transfer of data.

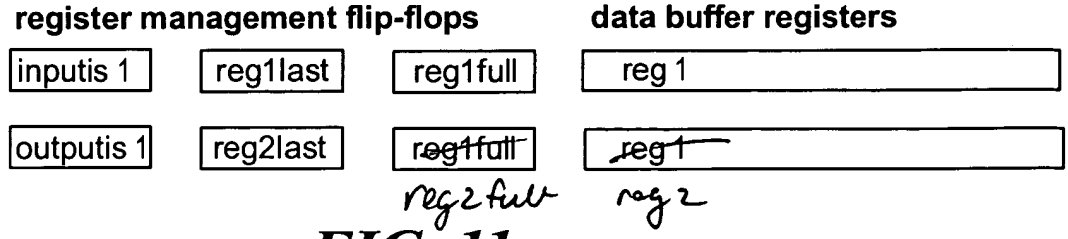

FIG. 11

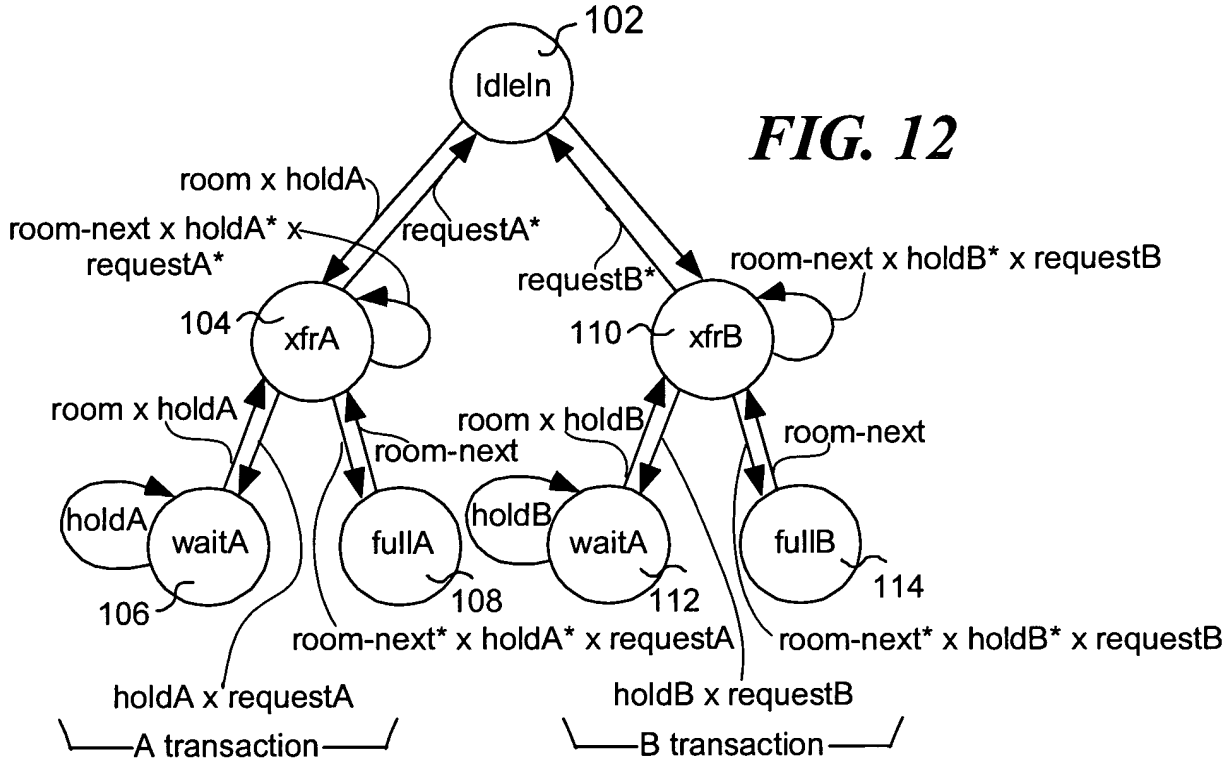

FIG. 12

transaction = IdleIn*
room-next = empty + xfr
room = reg1full* + reg2full + xfr
full = reg1full x reg2full
empty = reg1full* x reg2full*

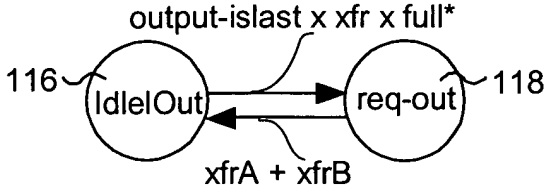

FIG. 13

FIG. 14

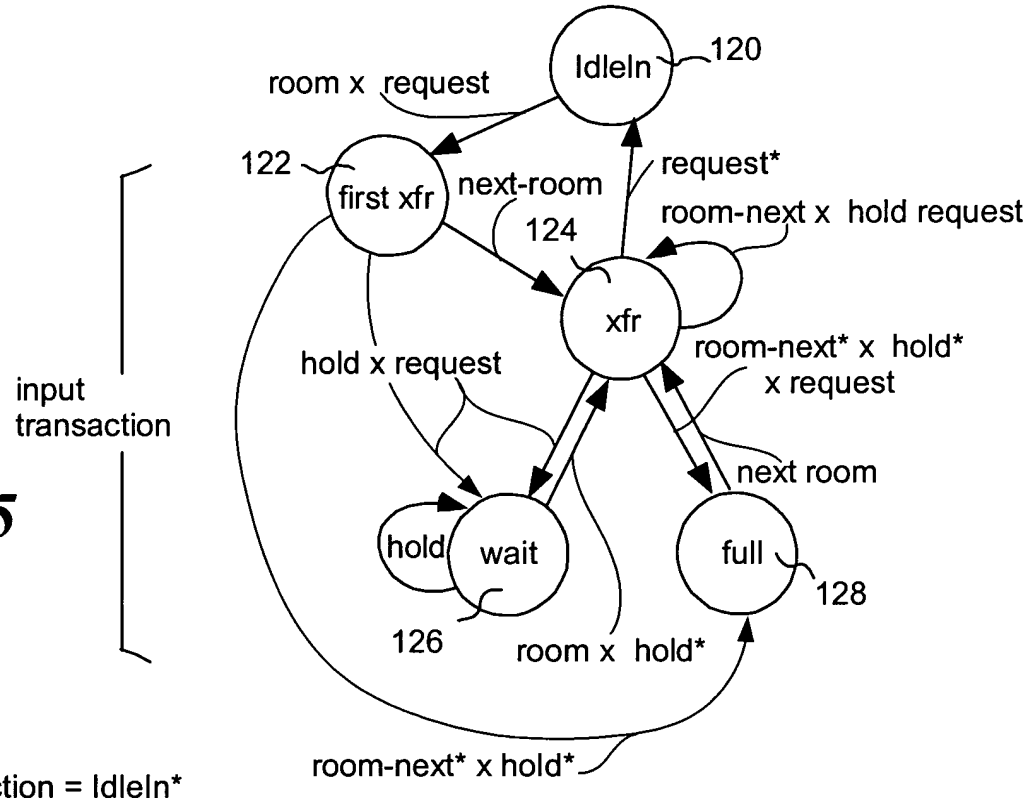

FIG. 15

transaction = IdleIn*
room-next = empty + xfrA + xfrB
room = reg1full* + reg2full* + xfrA + xfrB
full = reg1full x reg2full
empty = reg1full* x reg2full*

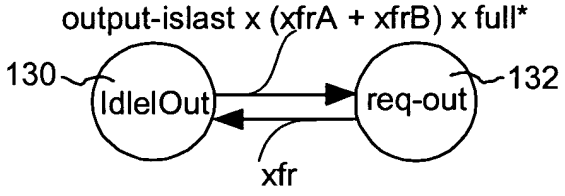

FIG. 16